REMARKS

The attached substitute specification contains no new matter as is apparent from the enclosed "Version With Marked Changes Made".

The amendments to the "Abstract" and "Claims" are reflected in the attached "Versions With Marked Changes Made."

Action on the merits is awaited.

Respectfully submitted,

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Version With Marked Changes Made

SPECIFICATION

SUBSTITUTE SPECIFICATION

FIELD OF THE INVENTION

[0001] The present invention relates to synchronization of transmitted signals. In particular, the present invention relates to synchronizing signals transmitted to a reception unit by a transmission unit.

BACKGROUND OF THE INVENTION

~~The present invention relates to a synchronization method for a reception unit, where cyclically emitted synchronization signals are transmitted to the reception unit by a transmission unit, where the reception unit supplies the synchronization signals to a first clock transmitter, where the first clock transmitter outputs an essentially stable number of clock signals between two synchronization signals, and also a reception unit corresponding thereto.~~

[0002] ~~Such synchronization methods and the corresponding~~**Reception units, and methods for synchronizing signals are generally known. These known** reception units~~are known generally. They~~ are used, among other things, in fieldbus systems, e.g. in the PROFIBUS. Such fieldbus systems are distributed control systems which generally have a transmission unit (head assembly, bus master) and a multiplicity of reception units (slaves). The individual slave assemblies are usually driven by virtue of the transmission unit transmitting an instruction message to the

reception units. Upon receipt of the instruction message, the reception units output to a controlled technical installation nominal values which have been transmitted to them previously by the transmission unit. At the same time, they read in from the controlled technical installation actual values which they subsequently transmit to the transmission unit. The transmission unit then calculates new nominal values which it transmits to the individual reception units, so that the reception units are ready for the next instruction message.

[0003] The instruction messages are sent by the transmission unit with equidistant timing. From the instruction messages it is therefore possible to derive synchronization signals which can be used to synchronize the reception units to the transmission unit.

[0004] In practice, some latitude in time remains between transmission of the actual values read ~~in to~~**into** the transmission unit and transmission of the nominal values to the reception units, on the one hand, and transmission of the next instruction message, on the other hand. This latitude is generally used for "acyclic" messages. In this context, delays by the acyclic messages may cause individual instruction messages to be sent late. Reception of such instruction messages sent late causes erroneous resynchronization of the reception units. ~~In many applications, this erroneous resynchronization is not critical.~~

[0005] In time-critical applications~~, on the other hand~~, particularly when coupling interpolating drive axes, such erroneous resynchronization cannot be tolerated. To prevent it, a phase regulator has therefore been proposed such that the reception unit supplies the synchronization signals to ~~the~~**a** first clock transmitter via this phase regulator in a phase locked loop, and, upon receipt of the synchronization signals, the phase regulator ascertains instantaneous phase errors and readjusts the first clock transmitter such that the first clock transmitter outputs a nominal number of clock signals between two synchronization signals. To achieve sufficient accuracy in the synchronization with the transmission unit, it has been proposed that the phase regulator integrate the instantaneous phase errors to form an integration value, and that the integration value be corrected to form an integration fraction, the integration fraction being less than one ~~(cf.~~ **This method is described in foreign patent application** DE 19932635.5~~)~~ **which is herein incorporated by reference**.

[0006] The phase regulator in the phase locked loop (PLL) generates a stable clock signal essentially from a synchronization signal which is received via the fieldbus system and is subject to interference. If this synchronization signal received via the fieldbus system disappears permanently~~,~~ ~~(~~e.g. **because there is** no bus connection available any longer~~)~~, then the phase regulator continues to produce a stable clock signal, although without being able to synchronize itself to the synchronization signal on the fieldbus system.

[0007] If the synchronization signal received via the fieldbus is permanently available again after some time~~,~~ ~~(~~e.g. bus connection restored~~)~~, this synchronization signal will generally be entirely asynchronous with respect to the stable clock signal produced by the phase regulator. ~~If~~ **In this case, if** the phase regulator is stopped ~~in this case~~, the stable clock pulses produced by the PLL disappear. If the phase regulator is restarted again, the stable clock pulses produced by the PLL are again produced in ~~synchronisms~~**synchronization** with the synchronization signal received via the fieldbus.

[0008] This conventional procedure is ~~problematical, however,~~**problematic** in terms of **the** requirements of various applications, such as the coupling of interpolating drive axes. The synchronous operation of various axes, e.g. in the case of numerically controlled machine tools or robots, is dependent on the stable clock signal produced by the PLL. ~~Actual~~ **For example, actual** values are stored in synchronism with this clock pulse~~, for example,~~ and nominal values are output.

[0009] ~~However, the~~**The** result of the disappearance of the clock signal produced by the PLL is ~~then~~ that the machine tool is no longer able to determine the position of its axes and that the machine operator needs to ~~rereference~~**re-reference** his axes. **For this reason, it is desirable, from an application point of view, for resynchronization to be able to be carried out without the stable clock pulses produced by the PLL disappearing.**

[0010] ~~For this reason, it is desirable, from an application point of view, for resynchronization to be able to be carried out without the stable clock pulses produced by the PLL disappearing.~~

[0011] Accordingly, **what is need is a** resynchronization to the synchronization signal received from the fieldbus ~~should be~~ **which is "**soft**"**, i.e. should involve only a slight change in the stable clock signal produced by the PLL.

SUMMARY OF INVENTION

[0012] It is the object of the present invention to provide a synchronization method for a reception unit which allows soft synchronization to an astable clock system, and also a reception unit corresponding thereto.

[0013] ~~The present invention achieves this object by developing the synchronization method described in the introduction on the basis of the preamble of the main claim, such that~~

[0014] ~~— the stable clock signals are used to drive a second clock transmitter,~~

[0015] ~~— where the second clock transmitter generates a second clock signal which is continuously present, even when the first stable clock signals are absent,~~

[0016] —**The present invention achieves this object by driving a second clock transmitter with stable clock signals, where the second clock transmitter generates a second clock signal which is continuously present, even when the first stable clock signals are absent and** where a phase difference arising between the

first clock transmitter and the second clock transmitter is compensated for by influencing the period duration of the second clock transmitter.

[0017] The result of soft synchronization is that the clock signals produced largely keep their period duration, so that there is ~~the~~ assurance that applications called cyclically with this timing, such as software applications, can also be executed to the full extent. Since the clock signals largely maintain their period duration, the application also remains sufficiently accurate. **In** ~~Particularly~~**particularly,** at points where timing is critical, such as speed calculations etc., great advantages are obtained ~~here~~**by the present invention** as compared with a closed loop control solution. The **net result being that the** process of soft synchronization ~~thus~~ barely differs from the normal operating state of the machine.

[0018] In ~~this context, it has been found to be~~**accordance with the present invention, it is** advantageous if only slight changes in the period duration of the second clock transmitter are made such that the phase difference is continuously reduced within a prescribed time period until the first and the second clock signal are synchronous with one another. In this way, the process of synchronization is particularly soft. **Thus, synchronization is performed particularly effectively if the period duration of the second clock transmitter is influenced such that the shorter interval between the phases of the two clock signals is reduced.**

[0019] ~~Synchronization is performed particularly effectively if the period duration of the second clock transmitter is influenced such that the shorter interval between the phases of the two clock signals is reduced.~~

[0020] In accordance with another ~~advantageous refinement of the method according to~~**embodiment of** the present invention, the second clock transmitter is driven with a prescribed standard period duration in the event of the first stable clock signal being absent. This ensures that, even if the synchronization signal disappears, autarchic operation of the application is possible.

[0021] When a phase regulator~~, outlined in the introduction~~ **of a conventional system, as described above**, in a locked loop (PLL) is used to produce a first stable clock signal, the invention can be implemented particularly simply and effectively if fluctuations in the period duration of the first clock transmitter which are corrected by the phase regulator are mapped onto the second clock transmitter.

[0022] In this context, it has been found to be beneficial if the corrections in the period duration of the first clock transmitter which are ascertained by the phase regulator from clock pulse to clock pulse are taken into account both in the first stable clock signal and in the continuously present second clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] ~~Other~~**For a complete understanding of the present invention and the** advantages ~~and details of~~**thereof, reference is now made to** the ~~invention can be~~

~~found in the~~**following** description ~~below of an advantageous exemplary embodiment~~ ~~and~~**taken** in conjunction with the ~~figures. In these, elements having the same functionality are identified using the same~~**accompanying drawings in which like** reference ~~symbols. The figures show basic illustrations, in which~~**numbers indicate like features, components and method steps, as wherein:**

[0024]

~~DRAWINGS~~

~~Figure 1 shows~~**FIG. 1 illustrates** a distributed control system~~,~~**;**

~~Figure 2 shows~~**FIG. 2 illustrates** a reception unit~~,~~**;**

~~Figure~~**FIG.** 3~~shows~~ **illustrates** a phase locked loop with a controlled clock transmitter connected downstream~~,~~**;** and

~~Figure 4 shows~~**FIG. 4 illustrates** a timing diagram for the controlled synchronization.

DETAILED DESCRIPTION OF THE INVENTION

[0025] ~~In accordance with FIGURE 1,~~**Now referring to the drawings, FIG. 1 illustrates** a distributed control system ~~has~~**. The distributed control system includes** a transmission unit 1 and reception units 2 connected to one another by means of a bus system 3. The transmission unit 1 cyclically transmits messages to the reception units 2, which react to the received messages accordingly. By way of example, the reception units 2 read in input variables from a controlled technical

installation or application 4, and emit output variables to the technical installation or application 4. This is indicated in ~~FIGURE~~**FIG.** 1 by the arrows between the reception units 2 and the technical installation/application 4.

~~Usually, the transmission unit 1 and the reception units 2 communicate on the basis of the following, cyclically executed scheme:~~

[0026] **Usually, the transmission unit 1 and the reception units 2 communicate on the basis of the following, cyclically executed scheme:** First, the transmission unit 1 transmits to the reception units 2 output variables which are intended to be output to the technical installation/application 4. It then transmits an instruction message to the reception units 2. On transmission of the instruction message, the reception units 2 output the output variables to the technical installation 4 and read in input variables from the technical installation 4. The input variables read in are then requested by the transmission unit 1.

[0027] Ideally, the above scheme is executed strictly cyclically and with strictly equidistant timing. In particular, the instruction messages can therefore be used as synchronization signals "S," or synchronization signals "S" can be derived from the instruction messages. The synchronization signals "S" can then be used to synchronize the reception units 2 to the transmission unit 1.

[0028] On the basis of ~~FIGURES~~ **FIGS.** 2 and 3, the synchronization signals received by the reception units 2 are supplied via a bus connection module 2' to a

phase regulator 5 in a phase locked loop 6. The phase locked loop 6 has a clock transmitter 7. Within the clock transmitter 7, a clock generator 8 produces primary clock signals which are supplied to a frequency divider 9. At the output, the frequency divider 9 outputs the divided primary clock signals as **individual** clock signals. The clock signals are supplied to a clock signal counter 10.

[0029] ~~With ideal regulation of the clock generator 8, the clock transmitter 7 outputs exactly one nominal number Z* of clock signals between two synchronization signals S. However, the clock transmitter 7 generally outputs a number Z of clock signals which differs from the nominal number Z*. The phase regulator 5 therefore ascertains instantaneous phase errors z upon receipt of the synchronization signals, and then readjusts the clock transmitter 7 such that it outputs the nominal number Z* of clock signals between two synchronization signals S. This is done as follows:~~

[0030] **With ideal regulation of the clock generator 8, the clock transmitter 7 outputs exactly one nominal number Z* of clock signals between two synchronization signals "S." However, the clock transmitter 7 generally outputs a number Z of clock signals which differs from the nominal number Z*. The phase regulator 5 therefore ascertains instantaneous phase errors z upon receipt of the synchronization signals, and then readjusts the clock transmitter 7 such that it outputs the nominal number Z* of clock signals between two synchronization signals "S." This is done as follows:** Before the start of synchronization, ~~that is to say~~**in other words** before the first instantaneous phase error z is ascertained, a control unit 11 first prescribes a start signal for a driving unit

12. This driving unit then drives the clock generator 8 in the clock transmitter 7. When the clock signal counter 10 has counted the nominal number Z* of clock signals, the clock signal counter 10 transmits a signal to the driving unit 12. The driving unit **12** then stops the clock generator 8 again. The phase locked loop 6 has thus been "biased", so to speak. Upon receipt of the next synchronization signal, which is likewise transmitted to the driving unit 12, the driving unit then starts the clock generator 8 again. This increments the clock signal counter 10 again.

[0031] The reaching of the nominal number Z* and the arrival of the next synchronization signal "S" are reported to a primary clock counter 13. Upon the arrival of the first of these two signals, the primary clock counter 13 is started~~; upon~~. **Upon** the arrival of the second of the two signals, it is stopped. The count (which has an arithmetic sign) of the primary clock counter 13 is thus a direct measure of the error between the clocking of the clock transmitter 7 and the periodicity of the synchronization signals "S."

[0032] Upon receipt of the first synchronization signal "S" after the clock transmitter 7 has been restarted, the count of the primary clock counter 13 is transmitted to the control unit 11. The control unit uses it to calculate a correction value for driving the clock generator 8, and prescribes this correction value directly to the phase regulator 5. This at least substantially corrects the instantaneous phase error z detected during the first synchronization cycle.

[0033] In the further synchronization cycles, the primary clock counter 13 is always controlled on the basis of the synchronization signal "S" and the reaching of the nominal number Z*. The primary clock counter 13 is started upon the arrival of the first of these two signals and is stopped upon the arrival of the second of these two signals. The count of the primary clock counter 13 is supplied to a comparator 14.

[0034] The count on the primary clock counter 13 is compared with a maximum error. If the count exceeds the maximum error, a timeout counter 15 is incremented. In this case, no error signal is output to the phase regulator 5. The phase regulator 5 maintains its previous output signal.

[0035] The primary clock counter 13 is usually started and stopped whenever a synchronization signal "S" is transmitted. However, it is also possible for a validity signal "G" to be additionally transmitted to the phase locked loop 6 by the control unit 11. In this case, the primary clock counter 13 is started and stopped only if the validity signal "G" is present. It is also possible to start and to evaluate the primary clock counter 13 with a phase offset with respect to the synchronization signal "S."

[0036] If the phase regulator corrects the instantaneous phase errors to form a proportional fraction, with the proportional fraction being less than one, the phase error is corrected more ~~quickly.~~ **expeditiously.** This applies particularly when the proportional fraction is greater than the integration fraction.

[0037] If the phase regulator readjusts the clock transmitter only when the absolute value of the instantaneous phase error does not exceed a maximum error, delays in the synchronization signals as a result of acyclic messages do not cause erroneous readjustment of the clock transmitter.

[0038] If a counter is incremented when the maximum error is exceeded, it is possible to detect a permanent error in the communication between transmission unit and reception unit, in particular.

[0039] If a control unit transmits a validity signal to the phase locked loop, and the synchronization method is carried out only when the validity signal is present, it is necessary to ensure that the correct synchronization signals are used for synchronization.

[0040] If a clock generator within a clock transmitter produces primary clock signals which are supplied to a frequency divider whose output emits the divided primary clock signals as clock signals, it is certain that all the components arranged between the clock generator and the frequency divider are likewise synchronized in the correct phase.

[0041] If, before the first instantaneous phase error is ascertained, the clock transmitter outputs the nominal number of clock signals, is then stopped and is restarted upon receipt of the next synchronization signal, the reception unit is synchronized particularly rapidly upon startup.

[0042] If, upon receipt of the first synchronization signal after the clock transmitter has been restarted, the instantaneous phase error is at least essentially corrected and integration of the instantaneous phase errors and correction of the integration value, and possibly also correction of the instantaneous phase error, are not carried out until after receipt of the second synchronization signal, synchronization at the start of the method is speeded up even further.

[0043] ~~According to~~**In accordance with** the **present** invention, ~~however,~~ the stable clock signal Z produced by the phase regulator in the phase locked loop 6 (PLL) is used only as an intermediate signal "b." For the actual application 4 operated on the bus system 3 by the reception unit 2, another continuously present clock signal "a" is produced. This is done using a further clock transmitter 7' which~~, like the first clock transmitter 7, [lacuna] likewise via a clock generator 8' for producing~~ **produces** second primary clock signals and a frequency divider 9' connected downstream. The output signals therefrom are applied to a clock signal counter 10' connected downstream. The way in which these components work is thus essentially equivalent to that for the phase locked loop 6.

[0044] The intermediate signals "b" at the output of the first clock counter 10 in the phase locked loop 6 and the continuously present second clock signals "a" at the output of the further clock counter 10' are supplied to a further comparator "A" for ascertaining the difference between the clock signals "a" for the application 4 and the stable clock signals "b" from the phase locked loop 6. As the measurement result,

the difference "c" is supplied to a reporting unit C as a measure of the phase difference between the two clock signals "a" and "b." This reporting unit reports when "c" becomes zero, which means that the clock signal "a" for the application 4 is synchronous with the phase locked loop 6 and hence with the synchronization signal of the bus system 3.

[0045] In addition, the phase difference "c" is passed to a control unit B. This control unit additionally receives the regulator output "d" of the phase regulator 5 and also a status signal "e." The status signal "e" delivers information relating to the state of the phase locked loop 6, whether the PLL is locked and stable, or else not locked, astable, turned off or during the startup phase. A further signal "f" passed to the control unit B provides the request for "soft" synchronization when needed.

[0046] The following manner of operation is now selected for the control unit B:

- If the status signal "e" signals that the PLL 6 is not stable (not locked, turned off, startup phase etc.), the clock generator 8' is driven with a prescribed standard period duration. The clock generator 8 thus runs decoupled from the PLL 6 and allows the application 4 to continue to operate autonomously without interruption.

- If, by contrast, the status signal "e" signals that the PLL 6 is stable or locked, the clock generator 8' is driven using the regulator output "d" of the phase regulator 5, i.e. like the phase locked loop 6. The clock signals "a" and "b" are thus produced exactly equally, i.e. the phase difference "c" remains constant even if the clock signal "b" has slight fluctuations in period duration.

If the comparator A detects a phase difference "c" between the first clock signal "b" and the second clock signal "a," which is continuously present, for the application 4, the request signal "f" is used to ask the control unit B to drive the clock generator 8' with a value which is slightly modified as compared with the regulator output "d," so that the phase difference "c" is gradually reduced.

[0047] The slight change in the period duration of the clock signal "a" produced for the application 4 enables said clock signal "a" to be altered such that the phase difference "c" between the stable clock signal "b" produced by the PLL 6 and the clock signal "a" produced for the application 4 is slowly ("softly") reduced until, after a certain time, the two clock signals "a, b" are synchronous or have been synchronized with one another. For this purpose, the phase regulator 5 needs to be turned on (again), i.e. needs to produce clock pulses. By continuously measuring a phase difference between the stable clock signal "b" produced by the PLL 6 and the clock signal "a" produced for the application 4, this phase difference can be gradually equalized to zero at any time by specifically changing the period duration of the clock signal "a" produced for the application 4.

[0048] If the phase difference is +1000 ns, for example, then the period duration is now shortened by 10 ns in each case, for example in 100 periods of the clock signal "a" produced for the application 4. This slowly and gradually reduces this phase difference to zero (""soft synchronization"").

[0049] Turning off the stable clock signal "b" produced by the PLL 6 and turning it on again thus has no effect on the clock signal "a" produced for the application 4. The application 4 can be operated without interruption.

[0050] If, as in ~~the~~**an** exemplary embodiment **of the present invention,** the first clock transmitter 7 is regulated by means of a phase locked loop 6, it is necessary to ensure that the measured phase difference "c" does not alter from measurement to measurement on account of the control response of the PLL 6, so that the control unit B can drive the second clock transmitter 7' such that the phase difference "c" can be reduced specifically.

[0051] ~~To achieve this, the fluctuations in the period duration of the stable clock signal b produced by the PLL 6 are also - on account of the unavoidable control response of the PLL 6 - mapped in the clock signal a produced for the application 4, provided that the phase regulator 5 is not currently turned off~~

[0052] **To achieve this, the fluctuations in the period duration of the stable clock signal "b" produced by the PLL 6 are also mapped in the clock signal "a" produced for the application 4, due to the unavoidable control response of the PLL 6, provided that the phase regulator 5 is not currently turned off.** This means that the corrections in the period duration which are ascertained from clock pulse to clock pulse by the PLL 6 are taken into account both in the stable clock signal "b" produced by the PLL 6 and in the clock signal "a" produced for the application 4.

The phase difference "c" thus remains constant if the control unit B forwards only the regulator output "d" to the second clock transmitter 7'.

[0053] This relationship is shown in the illustration in ~~FIGURE~~**FIG.** 4. To this end, various cases X, Y and Z are shown, with the following signals being plotted above one another: received synchronization signal "S," stable clock signal "b" produced by the PLL 6 and clock signal "a," which is continuously present and is produced for the application 4.

[0054] Case X shows a situation in which the synchronization signal "S" is subject to slight jitter z (deviations from the ideal expected clock instant). This is indicated by virtue of the actual clock signal (unbroken line) being situated slightly to the side of an ideal expected clock instant (shown dotted). The stable clock signal "b" generated by the PLL 6 is then situated virtually exactly at the expected clock instant. The clock signal "a" produced for the application 4 is then situated to the side of the ideal exact clock instant with a possibly constant phase difference "c0."

[0055] In case Y1 or Y2, the synchronization signal "S" has a large degree of jitter z. This means that the PLL 6 produces a severe internal control response d1 or d2 in order to generate a clock signal "b" which is synchronous with the synchronization signal "S. " This would now have a negative effect on the clock signal "a" shifted by a phase difference "c," because the control response of the PLL 6 would mean that this phase difference "c" would not remain constant, but instead

would also change on the basis of the control response of the PLL 6. However, since the control unit B takes the regulator output "d" into account when driving the second clock transmitter 7', the phase difference "c" remains constant C0. The PLL control response thus changes over to the application clock signal "a."

[0056] By virtue of the oscillations at the regulator output "d" now being mapped onto the final clock signal "a" for the application 4 in cases Y1 and Y2, this clock signal "a" now behaves in exactly the same way as the first clock signal "b" from the PLL 6. This produces a defined phase difference "c" between the clock signals "a" and "b." The two clock signals "a, b" thus appear identical and are shifted in time with respect to one another merely by a fixed phase shift. On the basis of these clock signals, the ""soft synchronization"" described above can then take place without difficulty.

[0057] In principle, the problem can also be solved by virtue of the clock signal "a" produced for the application 4 being regulated directly to the received clock signal "b" or to the synchronization signal "S." However, this has the following disadvantages:

- The "soft synchronization" needs to be carried out in the controlled variable of the regulator 5 (=**equals** corrections ascertained by the PLL) by a limiter. This nonlinearity complicates the control loop. ~~Said~~ **This** nonlinearity needs to be

examined on the basis of closed loop control technology and taken into account in the control loop (e.g. using additional limiters in the integral component of the regulator).

- In the application instance for a PROFIBUS, the PLL 6 is designed for correcting phase differences of approximately 1 µs (order of magnitude of the maximum jitter). The control parameters of the PLL 6 are therefore set very slowly or "softly" in order to filter the jitter. **However,** ~~The~~**the** phase shifts "c" arising during "soft synchronization" are situated in the ms range~~, however~~. This means that other, faster and hence "harder" control parameters would be needed first. Changeover between these two control parameter sets would again represent a further nonlinearity in the control loop, which in turn complicates the control loop. This would again need to be examined on the basis of closed loop control technology, and the necessary consequences would need to be derived.

- On the basis of closed loop control technology, it would be necessary to take account of the fact that the phase differences "c" are situated in the order of magnitude of the clock period durations. Depending on the control response, the two clocks under consideration could "overtake" one another, which could result in jumps in the phase difference measurement A. This in turn represents a nonlinearity whose consequences would need to be examined.

[0058] All these points represent increased levels of involvement with no advantage as compared with the open loop control solution in accordance with the

present invention. Reducing the problem to an open loop controller instead of a closed loop controller allows significant simplification by contrast.

[0059] The method according to the **present** invention allows~~, in particular,~~ even interpolating axes with distributed control to be driven with sufficient accuracy.

[0060] Although the present invention has been described in detail with reference to specific exemplary embodiments thereof, various modifications, alterations and adaptations may be made by those skilled in the art without departing from the spirit and scope of the invention. It is intended that the invention be limited only by the appended claims.

Version With Marked Changes Made

IN THE CLAIMS:

Please amend claims 1-7 as follows:

1. **(Amended)** A synchronization method for a reception unit ~~(2)~~, **said method comprising:**

~~where cyclically emitted~~**transmitting** synchronization signals ~~(S) are transmitted to the reception unit (2) by~~**from** a transmission unit ~~(1), where the~~**to at least one** reception unit ~~(2) supplies the~~**;**

supplying said synchronization signals ~~(S)~~**from said at least one reception unit** to a first clock transmitter ~~(7)~~, ~~where the~~ **said first** clock transmitter ~~(7) outputs an essentially~~**outputting a** stable number of clock signals ~~(b or Z)~~ between two **of said** synchronization signals**;** ~~(S),~~**and**

~~wherein these stable clock signals (b or Z) are used to drive~~ **driving** a second clock transmitter ~~(7'), where the second clock transmitter (7') generates~~**using said stable clock signals, said second clock transmitter generating** a second clock signal ~~(a)~~ which is continuously present, even when ~~the first~~**said** stable clock signals ~~(b and Z)~~ are absent, ~~where~~ **wherein** a phase difference ~~(c)~~ arising between ~~the~~**said** first clock transmitter ~~(7)~~ and ~~the~~**said** second clock transmitter ~~(7')~~ is compensated for by influencing ~~the~~**a** period duration of ~~the~~**said** second clock transmitter ~~(7')~~.

2. **(Amended)** The ~~synchronization~~ method ~~for a reception unit as claimed in~~**of** claim 1, wherein only slight changes in ~~the~~**said** period duration of ~~the~~**said** second clock transmitter ~~(7')~~ are made such that ~~the~~**said** phase difference ~~(c)~~ is continuously reduced within a prescribed time period until ~~the~~**said** ~~first~~**stable** clock ~~signal (b or Z)~~**signals** and ~~the~~**said** second clock signal ~~(a)~~ are synchronous with one another.

3. **(Amended)** The ~~synchronization~~ method ~~for a reception unit as claimed in~~**of** claim 1 or 2, wherein ~~the~~**said** period duration of ~~the~~**said** second clock transmitter ~~(7')~~ is influenced such that ~~the~~**a** shorter interval between ~~the~~ phases of ~~the~~**said** ~~two~~**stable** clock signals ~~(a, b) is~~**and said second clock signal are** reduced.

4. **(Amended)** The ~~synchronization~~ method ~~for a reception unit as claimed in one~~ of ~~claims~~**claim** 1 ~~to~~**or** ~~3,~~**2,** wherein ~~the~~**said** second clock transmitter ~~(7')~~ is driven with a prescribed standard period duration in the event ~~of the~~**said** first stable clock ~~signal (b or Z) being~~**signals are** absent.

5. **(Amended)** ~~The synchronization~~**The** method ~~for a reception unit as claimed in one~~ of claims 1 ~~to 4, where the~~**or 2, wherein said at least one** reception unit ~~(2)~~ supplies ~~the~~**said** synchronization signals ~~(S)~~ to ~~the~~**said** first clock transmitter ~~(7)~~ via a phase regulator ~~(5)~~ in a phase locked loop ~~(6),~~.

~~where the phase regulator (5), upon receiving the synchronization signals (S), ascertains instantaneous phase errors (Z) and readjusts the first clock~~

~~transmitter (7) such that the first clock transmitter (7) outputs a nominal number (Z*) of clock signals between two synchronization signals (S), wherein fluctuations in the period duration of the first clock transmitter (7) which are corrected by the phase regulator (5) are mapped onto the second clock transmitter (7').~~

6. **(Amended)** The ~~synchronization~~ method ~~for a reception unit as claimed in~~**of** claim ~~5~~**9**, wherein ~~the~~ corrections ~~(d)~~ in ~~the~~**said** period duration of ~~the~~**said** first clock transmitter ~~(7)~~, which are ascertained by ~~the~~**said** phase regulator ~~(5)~~ from clock pulse to clock pulse, are taken into account both in ~~the first~~**said** stable clock signal ~~(b or Z)~~ and in ~~the continuously present~~**said** second clock signal ~~(a)~~.

7. **(Amended)** A reception unit for ~~carrying out a synchronization method as claimed in one of the preceding claims.~~**synchronizing signals, said reception unit comprising:**

~~Abstract~~

a first clock transmitter, said first clock transmitter outputting a stable number of clock signals between two of synchronization signals received from a transmission unit; and

a second clock transmitter, said second clock transmitter using said stable clock signals, said second clock transmitter generating a second clock signal which is continuously present, even when said stable clock signals are absent, wherein a phase difference arising between said first clock transmitter and said

second clock transmitter is compensated for by influencing a period duration of said second clock transmitter.

Version With Marked Changes Made

IN THE ABSTRACT:

Please amend the Abstract as follows:

ABSTRACT OF THE DISCLOSURE

~~Method~~**A method** for controlled synchronization to an astable clock system, and reception unit corresponding thereto **are disclosed.** Soft synchronization using a slight change in the period duration of the clock signal ~~(a)~~ produced makes it possible to alter said clock signal such that a phase difference ~~(c)~~ between the stable clock signal ~~(b)~~ produced by a ~~PLL (6)~~**phased locked loop** upon a synchronization signal ~~(S)~~ and the clock signal ~~(a)~~ produced for ~~the~~**an** application ~~(4)~~ is slowly reduced until the two clock signals ~~(a, b)~~ are in ~~synchronisms~~**synchronization** with one another after a ~~certain~~**period of** time. ~~This means that the clock signals a produced largely keep their period duration, so that there is the assurance that applications called cyclically with this clock pulse can be executed to the full extent with the necessary degree of accuracy. By virtue of fluctuations in the period duration of the first clock transmitter which are corrected by the PLL (6) being mapped onto the second clock transmitter, a phase difference (c) which is to be compensated for remains constant. The process of soft synchronization thus barely differs from the normal operating state.~~